

2814

PATENT
81788.0025

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re application of:

Seiichi Mori

Serial No: 09/451,619

Filed: November 30, 1999

For: NON-VOLATILE SEMICONDUCTOR MEMORY AND
MANUFACTURING METHOD THEREOFCommissioner for Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith is a Amendment and 2 new drawings in the above-identified application.

No additional fee is required.

The fee has been calculated as shown below:

	(Col. 1) CLAIMS REMAINING AFTER AMENDMENT		(Col. 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Col. 3) PRESENT EXTRA*	LG/SM \$ ENTITY FEE		ADD'L FEE DUE
TOTAL CLAIMS FEE	9	-	20	**	0	LG=\$18 SM=\$9	\$ 0
INDEPENDENT CLAIMS FEE	2	-	5	***	0	LG=\$80 SM=\$40	\$ 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIMS						LARGE ENTITY FEE = \$270 SMALL ENTITY FEE = \$135	\$
						TOTAL	\$ 0

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space. The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box on Col. 1 of a prior amendment or the number of claims originally filed.

A check in the amount of \$ 0 to cover the additional claims fee is enclosed. A copy of this sheet is enclosed.

A check in the amount of \$ 0 to cover the extension fee is enclosed. A copy of this sheet is enclosed.

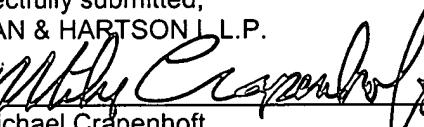
The Commissioner is hereby authorized to charge any deficiencies of fees associated with this communication or credit any overpayment to Deposit Account No. 50-1314. A copy of this sheet is enclosed.

Any filing fees under 37 C.F.R. § 1.16 for the presentation of extra claims

Any patent application processing fees under 37 C.F.R. § 1.17

Date: March 7, 2003

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Respectfully submitted,
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PATENT
81788.0025



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MORI, Seiichi

Serial No: 09/451,619

Filed: November 30, 1999

For: NON-VOLATILE
SEMICONDUCTOR MEMORY
HAVING A DECREASED GATE
LENGTH AND MANUFACTURING
METHOD THEREOF

AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Further to the Continued Prosecution Application (CPA) filed September 5, 2002, please amend the above-referenced application as follows:

IN THE SPECIFICATION:

• Please replace the paragraph at page 4, line 34 – page 5, line 3, with the following amended text:

C1
Further, in the case of the memory cell wherein the electric charge accumulating layer receiving the implantation of the hot electrons is defined as the trap level within the insulating layer, the erasing operation may involve pulling the electrons held by the trap level to the drain region by tunneling, or more preferably may involve

Art Unit: 2814
Examiner: WEISS, Howard

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
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